REMARKS

Claims 1-24 are pending to the present application. By virtue of this response, claims 1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, and 22 have been amended and no claim has been cancelled or added. Accordingly, claims 1-24 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as dedication to the public of any of the subject matter of the previously presented.

Information Disclosure Statement (IDS)

Applicants have submitted Chapters 3, 4, 6, and 8 of BSIM Pro+ Basic Operations and portions of the BSIM Pro Device Modeling Guide in the supplemental IDS filed together with this response to the outstanding Office Action. Applicants have attempted but failed to locate the entire BSIM Pro Device Modeling Guide. The original publisher of the document, Celestry Design Technologies, Inc., was no longer in business since late 2002. This document is not available from the website of Cadence Design Systems, Inc., the owner of Celstry Design Technologies, Inc. Applicants herein submit the portion of the BSIM Pro Device Modeling Guide that Applicants did find.

Claim Objections

Applicants have also amended claims 1, 5, 9, 13, 17, and 21 to remove the "if" statement. The support for the amended claims 1, 5, 9, 13, 17, and 21 is found in Figures 9B and 9C and their corresponding descriptions in paragraphs [0037] to [0039] from page 25 to 27 of the pending application.

Claim Rejection under 35 U.S.C. § 101

Claims 1-8, and 17-24 stand rejected under 35 U.S.C. 101 because the claimed inventions is directed to non-statutory subject matter.

"Only when the claim is devoid of any limitation to a practical application in the technological arts should it be rejected under 35 U.S.C. 101." (MPEP §2106(II)(A), emphasis added)

Under this test, "[a] claim is limited to a practical application when the method, as claimed, produces a concrete, tangible and useful result; i.e., the method recites a step or act of producing something that is concrete, tangible and useful." (MPEP §2106(IV)(B)(2)(b), part ii). For example: "transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces 'a useful, concrete and tangible result' – a final share price ...." (MPEP §2106(II)(A); citing State Street, 149 F.3d at 1373).

The Office alleges that claims 1-8, and 17-24 do not produce a concrete, useful, and tangible result. Applicants respectfully disagree. As one of ordinary skill in the art would recognize that "simulating the group of leaf circuit ..." as recited in Claims 1-8 and 17-24 generates predicted behavior of the circuit. Referring to Figures 1 and 3A of the present application, the simulation results (i.e., the predicted behavior) may be displayed, for example, in the form of waveforms 128, on a computer screen for engineers to inspect. These simulation results may be used to detect and correct design errors and to optimize design parameters, for example. Thus, similarly to the process in State Street, "simulating the group of leaf circuit ..." as recited in Claims 1-8, and 17-24 is a practical application in the technological arts because it transforms data (e.g., a netlist description of the circuit) into a useful, concrete, and tangible result - simulation results such as, for example, waveforms or measurements. In particular, these simulation results are useful, concrete, and tangible in the same sense as was the final share price (a calculated number) cited in State Street.

In addition, claims 1-8, and 17-24 also describes "creating a first port connectivity interface dynamically for the group of leaf circuits...". The port connectivity interface is a data structure used in the simulation. In *In re Warmerdam*, 33F.3d 1354, the Federal Circuit held that "Applicant's data structures are physical entities that provide increased efficiency in computer operation. More than mere abstraction, the data structures are specific electrical or magnetic structural elements in a memory." Applicants submit that the data structure of the present invention provides tangible benefits: it efficiently communicates changes in signal conditions among the group of leaf circuits.

Hence, Applicants respectfully request that the Office withdraw the rejection under 35 U.S.C. 101.

Claims 17-24 stand rejected under 35 U.S.C. 101 because the claimed inventions is directed to non-statutory subject matter.

In response, Applicants submit that claims 17-24 do explicitly include a medium for storing computer programs, which is the memory described in claim 17. In addition, claim 17 also requires that the simulator module (a computer program) is used in conjunction with at least a processing unit (CPU), a user interface, and a memory, all of which are shown in Figure 7 of the pending application.

Double Patenting

Claims 1-24 stand rejected on the ground of nonstatutory double patenting over claims 1-18 of U.S. Patent No. 7,024,652 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent. Applicants respectfully traverse this rejection.

In response, Applicants respectfully submit that the claims of the pending application are significantly different from U.S. 7,024,652. First, U.S. 7,024,652 does not require the claim elements "creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit, wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and simulate the group of leaf circuits in accordance with the first port connectivity interface" as recited in the claims of the pending application. The Office Action cites a matrix operation of U.S. 7,024,652 that corresponds to these claim limitations, Applicants respectfully disagree. As recited in the pending claims, the port connectivity interface is a dynamically created data structure during simulation, which person skilled in the art would understand is different from the matrix of U.S. 7,024,652. The matrix is used for the purpose of computation, while the port connectivity interface is used for communicating changes in signal conditions among the group of leaf circuits.

In addition, Applicants submit that evaluating the isomorphic behavior of two or more leaf circuits as required by the pending claims is distinguished from determining the strength of coupling

between two or more leaf circuits as recited in U.S. 7,024,652. The claim of U.S. 7,024,652 examines the strength of coupling signals between two leaf circuits in order to determine the strength of couple between the two leaf circuits. On the other hand, paragraphs [0037] to [0039] of the specification describe the method for evaluating the isomorphic behavior of two leaf circuits. In particular, the method determines whether the two leaf circuits have 1) a substantially same set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits; 2) a substantially same set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and 3) a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals. For at least the reasons presented above, Applicants submit that the double patenting rejection should be withdrawn.

Claim Rejection Under 35 U.S.C. § 112

Claims 2, 6, 10, 14, 18, and 22 stand rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement.

In response, Applicants have amended claims 2, 6, 10, 14, 18, and 22 to replace the "observe by" language in these claims.

Claims 9-16 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being incomplete for omitting essential structural cooperative relationship of elements, such omission amounting to a gap between the necessary structural connections.

In response, Applicants have amended claim 9 to include the limitation of a simulator module. Claims 10-16, which variously depend from claim 9, therefore also include this limitation of the simulator module. The support for the amended claim 9 is found in Figures 7 and its corresponding descriptions from page 18 to 20 of the pending application.

Claims 2-3, 5-7, 10-11, 14, 17-19, and 21-23 stand rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response, Applicants have amended claims 2, 10, and 18 to clarify the meaning of "substantially same isomorphic behavior" and have amended claims 6, 14, and 22 to clarify the meaning of "substantially different isomorphic behavior." In each of the claims 2, 6, 10, 14, 18, and 22, Applicants further define the meaning of "substantially same" in the context of electrical signals that are within a predetermined threshold of signal tolerance. In other words, a person skilled in the art would understand that in order to determine whether two signals are substantially the same, a predetermined threshold of signal tolerance is used. If the two signals are within the predetermined threshold of signal tolerance, they are deemed to be substantially the same. On the other hand, if the two signals have deviated such that they are not within the predetermined threshold of signal tolerance, they are deemed to be not substantially the same (or substantially different). In practice, a person skilled in the art would understand that the predetermined threshold of signal tolerance may be programmed by designers as simulation parameters prior to the actual simulation. The support for the amended claims 2, 6, 10, 14, 18, and 22 is found at least in paragraphs [0037] to [0039]. Based on the above amendments and the support of paragraphs [0037]-[0039], Applicants submit that claims 2-3, 5-7, 10-11, 14, 17-19, and 21-23 are definite in view of 35 U.S.C. 112, second paragraph.

Claim Rejection under 35 U.S.C. § 102

Claims 1-24 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Tcherniaev (U.S. Patent No. 6,577,992).

In response, Applicants respectfully submit that the Tcherniaev reference does not disclose each and every element of the pending independent claims 1, 9, and 17. Specifically, the Tcherniaev reference does not disclose at least the elements "representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior; creating a first port connectivity interface dynamically for the group of leaf circuits in

response to the merged leaf circuit; wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits" of the pending independent claims.

Applicants submit that one of the key differences between the current invention and the Tcherniaev reference lies in how dynamic information among the circuit components under simulation is communicated and what data structure are used for communicating such dynamic information during a transient simulation. It is known in the art that during a simulation, the simulator needs to keep track of port connectivity information of the circuit components. It is also known that during a simulation, the circuit components will go through different dynamic states. So the issue is not whether the port connectivity information or dynamic states exist or not, but how are they stored or used by the simulator.

In the Tcherniaev reference, it chose to store such information in the static database while the current invention uses a newly created dynamic data structure called the port connectivity interface for storing and communicating such dynamic information during simulation. However, there is major design tradeoffs involved in each implementation approach. The pending application describes the Tcherniaev approach in Figure 6 and its corresponding paragraphs [0018] – [0020] in the background section of the specification. In particular, the Tcherniaev approach employs pointers to pass such dynamic information through the subcircuit instances (See Figure 2C of Tcherniaev.) Therefore, to pass information from one subcircuit to the next subcircuit in a different hierarchical branch, such as from subcircuit 620 to subcircuit 622 as shown in Figure 6 of the pending application, the simulator of the Tcherniaev reference would have to made multiple program calls (via the pointers). As indicated in the background section of the pending application, the problem with the method taught by Tcherniaev reference is that the dynamic information needs to traverse many levels of the hierarchical data structure before reaching its destination. At each hierarchical level, information needs to be synchronized before it may be transmitted to the next level, which the Tcherniaev reference are totally silent about these design issues. Therefore, the method of passing information through the hierarchies, as taught by Tcherniaev, and synchronizing at each intermediate level would result in lower simulation performance.

The Office Action cites column 4 lines 44-47, Fig. 2B-2D, and Fig. 3 allegedly teach these claim elements, Applicants respectfully disagree. Applicants respectfully submit that merely

mentioning the terms "port connectivity" does not indicate a particular approach used by the simulator. On the contrary, the Tcherniaev reference teaches a different approach for storing and handling dynamic information created during the simulation. For example, the Tcherniaev teaches that "[T]he static storage may therefore store the matrix structure. As described above, the static subcircuit storage 212 may further include a subcircuit definition 217 that defines the subcircuit topology. In addition, the static subcircuit storage 212 may provide element definitions 219 associated with the subcircuit definition 217." (See Tcherniaev, column 9, lines 50-55, emphasis added.) The Tcherniaev also teaches that "[I]t is important to note that the circuit simulation is advantageously accomplished by traversing a hierarchical data structure such as that illustrated in FIG. 2A without flattening the hierarchical data structure." (See Tcherniaev, column 10, lines 7-10, emphasis added.) The Tcherniaev further states that "[I]n addition to sharing an equivalent circuit structure and therefore static subcircuit storage, two subcircuit instances may have an equivalent dynamic voltage state obtained during transient simulation. As shown in FIG.2C, multiple instances 224, 226, 228 of the same subcircuit definition may share the same static subcircuit storage 212 as described above." The Tcherniaev reference further teaches that "one or more pointers ... may be used to permit both the first instance 224 and the third instance 228 to share this dynamic voltage state." (See Tcherniaev, column 10, lines 17-33, emphasis added.) Applicants also note that column 14 lines 39-54 and column 16 line 35 to column 17 line 47 of the Tcherniaev reference teaches updating rate of change in node voltage, again by using pointers to traverse the hierarchical data structure. It is clear that the Tcherniaev reference teaches storing dynamic simulation information in the static subcircuit storage and using pointers to traverse the hierarchical data structure for passing dynamic information among subcircuits under simulation. The Tcherniaev reference is totally silent about the design issues, such as multiple program calls and synchronization between hierarchies, associated with its approach. No dynamic data structure, such as the port connectivity interface, is created by the Tcherniaev reference in response to the isomorphic behavior of the group of leaf circuits under simulation. The present invention addresses these design issues by using the port connectivity interface to facilitate communication of dynamic information among circuit components under simulation.

For at least the reasons presented above, Applicants respectfully submit that the Tcherniaev reference does not disclose each and every element of the independent claims 1, 9, and 17. Applicants

also assert that claims 2-8, 10-16, and 18-23, which variously depend from their independent claims, are allowable for at least the reason that they depend from allowable independent claims.

With respect to claims 5, 13, and 21, Applicants respectfully submit that the Tcherniaev reference does not disclose at least the element "splitting the merged leaf circuits into two or more individual leaf circuits in response to the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors; creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits; wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits."

Based on the arguments presented above, Applicants have established that the Tcherniaev reference does not disclose the solution of creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit to address the situation when leaf circuits in a transient simulation are merged. For the same reasons presented above, the Tcherniaev reference does not disclose the solution of creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits to address the situation when a merged leaf circuit in a transient simulation are split into two or more individual leaf circuits.

In addition, in the response to the double patenting rejection, Applications have explained the differences between the concepts of isomorphic behaviors of the pending application from the concepts of coupling strength as relied by the Office Action in rejecting these claims.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 188122001700. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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